UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	Son K. Quan et al.	GROUP ART UNIT:	2831
APPLN. NO.:	09/928,737	EXAMINER:	Hung V. Ngo
FILED:	August 13, 2001	CONFIRMATION No.: 7252	
TITLE:	SEMICONDUCTOR PACKAGE AND METHOD THEREFOR		

Certificate of Submission
I hereby certify that this correspondence is being submitted to the USPTO, Alexandria, VA by submission via the EFS web system.
February 17, 2010
Date of Submission
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Signature
Pat Thomas
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APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent. Applicants previously paid the $540.00 Appeal Brief Fee by a charge to Deposit Account No. 503079 (Freescale Semiconductor, Inc.). Applicants request that the previously paid appeal brief fee be applied to this Appeal Brief, filed following another final rejection having a notification date of January 13, 2010. Applicants continue to authorize any required fees associated with this application to be charged to Deposit Account No. 503079 (Freescale Semiconductor, Inc.).

Table of Contents

REAL PARTY IN INTEREST

The present Application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., with its headquarters in Austin, Texas.

RELATED APPEALS AND INTERFERENCES

Appellant is unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-16, 18 and 19 have been canceled.

No claims are allowed or objected to.

Claims 17 and 20-30 are pending in the Application and are involved in this appeal.

Claim 17 was previously presented. Claims 20-22 are original. Claims 23-30 were added via Amendment on September 17, 2008.

Claims 17 and 20-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Tuttle et al. (U.S. Patent 5,612,513). The rejection of claims 17 and 20-30 is being appealed.

STATUS OF AMENDMENTS

Prior to filing a first Notice of Appeal on March 20, 2003, no amendments to the claims as originally presented on August 13, 2001 had been made. In response to the Decision on Appeal mailed July 23, 2008, an amendment in furtherance of an R.C.E. under 37 CFR 1.114 was filed on September 17, 2008. A second amendment in response to a first Office Action was filed on February 23, 2009. A final rejection was issued on June 08, 2009. An amendment to the specification providing a required reference of priority to a prior Application was filed on June 29, 2009. No further amendments have been filed. A notice of appeal was filed on August 7, 2009. A compliant Appeal Brief was filed on October 7, 2009. A final rejection was issued on January 13, 2010 responsive to Applicants' second amendment filed on February 23, 2009. No new ground of rejection was provided. Applicants responded by initiating a new appeal. A notice of appeal was filed on February 11, 2010.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 17 is a method claim directed to forming a semiconductor package.

Independent claim 17 recites an interconnect substrate having a plurality of substantially identical package sites arranged in an array. This recited feature is described at least at page 2, lines 20-30 and shown in FIG. 1, which shows a substrate 11 that includes package sites 13, 14, 16, 21, 22, 23 arranged in an array.

Independent claim 17 recites the plurality of sites being separated by a singulation space. This recited feature is described at page 2, lines 30-33 and shown as the space 17 in FIG. 1.

Independent claim 17 recites the interconnect substrate being a ceramic substrate or a printed circuit board substrate. This recited feature is described at page 3, lines 1-3.

Independent claim 17 recites mounting and interconnecting a semiconductor device within each site. This recited feature is described at least at page 2, lines 25-30 and shown in FIG. 2 with components 26 mounted onto an area 12 of a substrate.

Independent claim 17 recites overmolding a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space. This recited feature is described at least at page 4, line 20, and shown in FIG. 2, which shows the encapsulant 19 covering semiconductor devices 26 mounted to a plurality of sites 21, 16, 14, and 13 separated by singulation spaces 17.

Independent claim 17 further recites that the top surface of the encapsulant has a surface deviation of less than 0.13 millimeters across a surface of the continuous encapsulant. This recited feature is described at least at page 5, lines 28-30.

Dependent claim 20 recites singulating the plurality of package sites after overmolding. This recited feature is described at least at page 5, lines 20-24 and shown in FIG. 3, which shows a singulated package formed from a package site 13.

Dependent claim 21 recites that singulating comprises sawing through the encapsulant and the substrate along the singulation space. This recited feature is described at least at page 5, lines 17-20.

Dependent claim 22 recites a step of handling each packaged semiconductor device with automated pick and place equipment. This recited feature is described at least at page 6, lines 22-23.

Independent claim 23 is a method claim directed to forming a semiconductor package.

Independent claim 23 recites a method for making a packaged semiconductor device. An interconnect substrate that is either a ceramic substrate or a printed circuit board substrate is provided. This recited feature is described at least at page 3, lines 1-4.

Independent claim 23 recites a plurality of substantially identical package sites arranged in at least a four by four array. This recited feature is described at least at page 5, lines 31-32 and shown, in a cross-sectional view, in FIG. 2.

Independent claim 23 recites that the plurality of [singulation] sites are separated by a singulation space. This recited feature is described at least at page 2, line 30-33 and shown as the space 17 in FIG. 1.

Independent claim 23 recites mounting and interconnecting a semiconductor device within each site. This recited feature is described at least at page 3, line 20-23 and shown in FIG. 2 with components 26 mounted onto an area 12 of a substrate corresponding to package sites 21, 16, 14, and 13 (shown in FIG. 1).

Independent claim 23 recites a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space This recited feature is described at least at page 4, line 20, and shown in FIG. 2, which shows the encapsulant 19 covering semiconductor devices 26 mounted to a plurality of sites 21, 16, 14, and 13 separated by singulation spaces 17.

Independent claim 23 recites that the top surface of the encapsulant has a surface deviation of less than 0.13 millimeters across the top surface of the continuous encapsulant. This recited feature is described at least at page 5, lines 28-30.

Dependent claim 24 recites singulating the plurality of package sites after overmolding. This recited feature is described at least at page 5, lines 20-24 and shown in FIG. 3, which shows a singulated package formed from a package site.

Dependent claim 25 recites that singulating comprises sawing through the encapsulant and the substrate along the singulation space. This recited feature is described at least at page 5, lines 17-20.

Dependent claim 26 recites a step of handling each packaged semiconductor device with automated pick and place equipment. This recited feature is described at least at page 6, lines 22-23.

Independent claim 27 is a method claim directed to forming a semiconductor package.

Independent claim 27 recites a method for making a packaged semiconductor device. An interconnect substrate that is either a ceramic substrate or a printed circuit board substrate is provided. This recited feature is described at least at page 3, lines 1-4.

Independent claim 27 recites a plurality of substantially identical package sites arranged in an array. This recited feature is described at least at page 5, lines 31-33 and shown, in a cross-sectional view, in FIG. 2.

Independent claim 27 recites that the plurality of sites are separated by a singulation space. This recited feature is described at least at page 2, line 30-33 and shown as the space 17 in FIG. 1.

Independent claim 27 recites mounting and interconnecting a semiconductor device within each site. This recited feature is described at least at page 3, line 20-23 and shown in FIG. 2 with components 26 mounted onto an area 12 of a substrate corresponding to package sites 21, 16, 14, and 13 (shown in FIG. 1).

Independent claim 27 recites overmolding an encapsulant over the plurality of sites and the singulation space. This recited feature is described at least at page 4, line 20, and shown in FIG. 2, which shows the encapsulant 19 covering semiconductor devices 26 mounted to a plurality of sites 21, 16, 14, and 13 separated by singulation spaces 17.

Independent claim 27 recites that the top surface of the encapsulant has a surface deviation of less than 0.13 millimeters across the top surface of the continuous encapsulant. This recited feature is described at least at page 5, lines 28-30.

Dependent claim 28 recites singulating the plurality of package sites after overmolding. This recited feature is described at least at page 5, lines 20-24 and shown in FIG. 3, which illustrates a singulated package formed from a package site 13.

Dependent claim 29 recites that singulating comprises sawing through the encapsulant and the substrate along the singulation space. This recited feature is described at least at page 5, lines 17-20.

Dependent claim 30 recites a step of handling each packaged semiconductor device with automated pick and place equipment. This recited feature is described at least at page 6, lines 22-23.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1) Are claims 17 and 20-30 patentable under 35 U.S.C. 103(a) over U.S. Patent 5,612,513 to Tuttle et al. ("Tuttle")?

ARGUMENTS

Claims 17 and 20-30

Independent claims 17, 23 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tuttle. However, because Tuttle does not teach each and every element of the claims, the rejection relies on an argument that the untaught elements reflect discovery of optimum ranges. Appellants' arguments and affidavit evidence show that the properties of the package of the present invention and the problems solved are so distinct from those of Tuttle that the present invention can in no way reflect optimization of Tuttle's ranges.

The immediate two past Office Actions rejected claims 17, 23, and 27 as obvious in view of Tuttle. In so doing, the Patent Office admitted Tuttle does not disclose the limitation "wherein overmolding produces a top surface of the encapsulant which has a surface deviation of less than 0.13 millimeters across a surface of the continuous encapsulant." The rejection therefore relied on a legal argument that "it would have been obvious…to modify the flat surface encapsulant of Tuttle by employing a surface deviation less than 0.13mm." This argument is based on the principle stated in *In re Aller,* 105 USPQ 233 that "where the general conditions of a claim are disclosed in prior art, discovering optimum ranges involves only routine skill in the art." The application of this principle here is clear error because Tuttle fails to disclose the general conditions of the present invention. Consequently, the invention of Appellants' claims 17, 23 and 27 can not reflect the discovery of optimum or workable ranges by routine experimentation.

As evidence to rebut the USPTO's obviousness argument, Appellants submitted a §1.132 Declaration dated Feb. 23, 2009 from Michael B. McShane, a microelectronics packaging technologist and IEEE Fellow with over 40 years of microelectronics packaging experience. In the most recent Final Rejection, this evidence was deemed insufficient on the basis that Tuttle evidences that a substrate or circuit board is not inherently rigid. Appellants respectfully traverse this basis. Tuttle teaches a "flexible substrate" as evidenced from the second sentence of the Abstract and as repeatedly being described as "flexible" (See Col. 2, line 43; Col. 3, line 22; Col. 4, line 9; Col. 6, line 7; Col. 6, line 59; Col. 7, line 5, et al.). The rejection basis for Tuttle teaching a "printed circuit board" was the phrase "substrate 14 with a printed conductive trace" and Appellants were directed to Col. 4, lines 24-30. The recited "ceramic substrate" of claim 17 is inherently rigid as ceramic is a rigid material. Also, printed circuit boards are well known in the industry to be rigid (see Tuttle's background at Col. 1, line

28). The recited "printed circuit board" of claim 17 is not taught or suggested by the "flexible substrate" of Tuttle. Appellants hereby request that members of the Appeal Board consider this evidence when considering the following arguments.

Appellants' §1.132 Declaration dated Feb. 23, 2009 from Michael B. McShane was also stated in the most recent Final Rejection to be insufficient for not providing evidence that the flexible package of Tuttle et al. is problematic for pick and place equipment. Appellants respectfully submit that paragraph 8 of the §1.132 Declaration is evidence to be considered in the obviousness determination, and the evidence states that when a vacuum is used for picking and placing that flexbile packages can deform and cause electrical issues.

First, Tuttle fails to disclose general conditions of the recited claims because Tuttle teaches away from the "substrate" element of the present invention. Claims 17, 23 and 27 specify using "a ceramic substrate or a printed circuit board substrate," which are by their very nature rigid (§1.132 Declaration, paragraph 9). Tuttle in contrast teach at Col. 1, lines 26-28 that use of "a rigid substrate, such as a printed circuit board," is problematic. Tuttle's entire Specification teaches only flexible substrates. For example, the second sentence of Tuttle's Abstract states "a flexible substrate is formed with a plurality of electrical circuits." And, in each of the Tuttle embodiments at Col. 4, lines 8-10; Col. 6, lines 6-8; Col. 7, lines 3-5; and Col. 8, lines 20-21, the substrate is described as being flexible and made of a flexible material. Tuttle teach that flexibility is necessary, as stated at Col. 4, lines 8-9; Col. 6, line 8; "to allow the final product to remain flexible." Flexibility is required to accommodate odd configurations or to avoid breaking of the substrate. Tuttle's package is directed toward an application where the package can be bent or flexed in an end-user product. The substrates recited in Appellants' claims 17, 23, and 27 produce packages that are non-flexible and therefore subject to breaking in the applications proposed by Tuttle (see Col. 1, lines 32-35). Thus, the substrates used by the two packages are intended for two unrelated product applications, each with their own separate and distinct advantages, neither of which could be derived from the other by discovery of an optimum range.

Second, Tuttle fails to disclose general conditions of the recited claims because Tuttle is silent with respect to the encapsulant's surface deviation. Tuttle teach only how much encapsulant should be used to fill the cavity. Embodiments of Tuttle disclose an encapsulant can substantially fill the cavity, completely fill the cavity, need not fill the cavity, does not completely cover the components, or can be deposited with different thicknesses on different portions of the substrate, as described respectively at Col. 9, lines 47-49 and Col. 5, lines 39-46. Tuttle also teach that the cavity can be filled with sufficient encapsulant to give each enclosed

circuit [emphasis added] a substantially flat surface so "the resulting circuit is completely encapsulated" between the encapsulant and the substrate as disclosed both at Col. 6, lines 55-58 and Col. 7, lines 46-50. However, in embodiments of Tuttle that discuss flatness, Tuttle's concern is only with the flatness of the top surface of each enclosed circuit and not across the entire surface of a continuous encapsulant. Tuttle's "flat surface" references are specific only to those portions of the encapsulant actually overlying the circuit. No such qualification regarding surface flatness exists for regions adjacent to the circuit. It is clear from a detailed reading of Tuttle that the intent for including the "substantially flat top" and "completely encapsulated" language is merely to provide an indicator for determining when sufficient encapsulant has been used to cover the circuit.

Moreover, since Tuttle's final product is intended to be flexible, it will be subject to bending that will cause it to deform. Such bending will produce an added degree of surface deviation and create attendant problems for marking and pick-and-place package-handling equipment (§1.132 Declaration, paragraph 8). In contrast, Appellants' claims 17, 23, and 27 all recite substrates that are made with materials that are inherently rigid and resistant to such bending. Surface deviation on these products will be maintained. In sum, Tuttle is simply silent with respect to the surface planarity across the entire surface of the encapsulant. Nothing in Tuttle provides general conditions that would make the 0.13 millimeter surface deviation across the surface of the encapsulant a discovery of optimum or workable ranges by routine experimentation.

Third, Tuttle fails to disclose general conditions of the recited claims because it is silent with respect to use of overmolding to encapsulate components on the substrate. Tuttle instead only teaches pouring encapsulant into the cavity for each circuit (Col. 7, lines 37-38).

The rule of law from the CCPA decision *In re Aller*, 105 USPQ 233, relied upon to form the rejection's basis is untenable with respect to the recited differences between Tuttle and Appellants' claims 17, 23, and 27. The differences between Tuttle's package and Appellant's package are not differences in range. Further, the decision in *In re Aller* involved a prior art teaching of a specific temperature and a specific solution concentration. The Tuttle reference teaches no such specificity. Tuttle only teaches that under conditions where encapsulant is used to completely encapsulate each circuit, sufficient encapsulant should be used to give each enclosed circuit a substantially flat top (Col. 6, lines 55-61). This is an amount of encapsulant that will vary between products of differing circuitry heights. Additionally, unlike the facts of *In re Aller*, the criticality of the claimed "surface deviation of less than 0.13 millimeters across a

surface of the continuous encapsulant" has been shown by the evidence proffered in Appellants' §1.132 Declaration regarding this claim recital's importance for equipment handling and marking. In contrast, in *In re Aller*, the Court stated that no criticality of a claimed range was shown by the Appellants. For at least the foregoing reasons, Appellants respectfully submit that the facts presented in this Appeal significantly differ from the holding of *In re Aller.*

For at least the reasons set forth above, Appellants respectfully submit that the claims 17 and 20-30 of the present Application are allowable over the art cited during prosecution.

Respectfully submitted,
Son K. Quan

/Robert L. King/

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CLAIMS APPENDIX

Claims 1-16 (Canceled)

17. (Previously Presented) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate having a plurality of substantially identical package sites arranged in an array, the plurality of sites being separated by a singulation space and the interconnect substrate being a ceramic substrate or a printed circuit board substrate;

mounting and interconnecting a semiconductor device within each site; and

overmolding a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space, wherein overmolding produces a top surface of the encapsulant which has a surface deviation of less than 0.13 millimeters across a surface of the continuous encapsulant.

Claims 18 and 19 (Canceled)

20. (Original) The method of claim 17 further comprising the step of singulating the plurality of package sites after overmolding.

21. (Original) The method of claim 20 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

22. (Original) The method of claim 21 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.

23. (Previously Presented) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate that is either a ceramic substrate or a printed circuit board substrate having a plurality of substantially identical package sites arranged in at least a four by four array, the plurality of sites being separated by a singulation space;

mounting and interconnecting a semiconductor device within each site; and

overmolding a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space to produce a top surface of the encapsulant which has a surface deviation of less than 0.13 millimeters across the top surface of the encapsulant.

24. (Original) The method of claim 23 further comprising the step of singulating the plurality of package sites after overmolding.

25. (Original) The method of claim 24 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

26. (Original) The method of claim 25 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.

27. (Previously Presented) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate that is either a ceramic substrate or a printed circuit board substrate having a plurality of substantially identical package sites arranged in an array, the plurality of sites being separated by a singulation space;

mounting and interconnecting a semiconductor device within each package site; and

overmolding an encapsulant over the plurality of sites and the singulation space to have a top surface planarity deviation of less than 0.13 millimeters.

28. (Original) The method of claim 27 further comprising the step of singulating the plurality of package sites after overmolding.

29. (Original) The method of claim 28 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

30. (Original) The method of claim 29 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.

EVIDENCE APPENDIX UNDER 37 CFR 41.37(c)(1)(ix)

A declaration under 37 C.F.R. 1.132 from Michael B. McShane has been entered into the record and is attached. This evidence is currently being relied upon by Appellants regarding the grounds of rejections to be reviewed in this appeal.

1

DECLARATION UNDER 37 C.F.R. § 1.132

Dear Commissioner:

I, Michael B. McShane, a resident of the city of Austin in the State of Texas, hereby state and declare as follows:

FACTS

1. I am currently employed in Austin, Texas, by Freescale Semiconductor, Inc. the assignee of the pending application. I am a technologist for in Freescale's intellectual property licensing group and I specialize in packaging technologies and manufacturing methods.

2. In 1968 I earned a Bachelor of Science in Mechanical Engineering from the University of Texas at Austin. I am an IEEE Fellow and in 2003 received the IEEE Exceptional Technical Achievement Award. In 2001 I received the Microelectronics Packaging Technologist of the Year Award. I was the 2000 program chairman and the 2002 general chairman for the IEEE Electronic Component and Technology Conference. I am on the Board of Directors of the IEEE/CPMT Society. I have been a keynote speaker for the International Microelectronics and System Conference. I am a named inventor on more than thirty issued U.S. patent on electronic packaging and assembly technologies, one of which was recognized as Motorola's patent of the year in 2000.

3. From 1968 until 1976 I was employed by Hughes Aircraft Company, Newport Beach, California as a Microelectronic Process Engineer. From 1976 until 2004 I was employed by Motorola, Inc. in Austin, Texas as an electronics packaging technologist. From 2004 until the present, I have been employed in Austin, Texas by Freescale Semiconductor, a Motorola spin-off and the assignee of U.S. Serial No. 09/928,737.

STATEMENTS

4. Tuttle et al. (U.S. Patent 5,612,513) discloses substantial flatness only across each enclosed circuit (See Col. 6, line 56). Unlike the pending Quan application, Tuttle et al. is silent with respect to the surface planarity across the continuous encapsulant. This is because as shown in FIG. 4 Tuttle et al. is concerned only with the flatness of the top surface of each enclosed circuit.

5. Tuttle et al. teaches being able to use components of unequal heights as part of the individual enclosed circuits (See Col. 1, line 66 thru Col. 2, line 1). Tuttle et al. teaches using enough encapsulant such that each enclosed circuit has a substantially flat top surface (See Col. 6, lines 55-57). This ensures that the tallest component is covered by the encapsulant (See Col. 6, lines 34-36 thru Col. 6, lines 55-57). Thus, substantial flatness is merely an indicator to ensure that only the necessary amount of encapsulant is used. Moreover, the only time Tuttle et al. mentions substantial flatness of the top surface of an enclosed circuit, it does so only in the context of ensuring that the tallest component of the enclosed circuit is covered by the encapsulant.

6. Tuttle et al. teaches pouring encapsulant into the cavity for each circuit (See Col. 7, lines 37-38). Tuttle et al. is silent with respect to overmolding.

7. Tuttle et al. has a flexible substrate to allow the final/finished product, a single package, to remain flexible (See Col. 2, lines 13-17, Col. 4, lines 8-10, Col. 6, lines 6-8 and Col. 7, lines 3-5). In order for the final product to remain flexible, the overlying encapsulant must also be flexible (See Col. 2, lines 24-27). Indeed, if the overlying encapsulant were not flexible, then Tuttle's final product would not be flexible.

8. Using automated pick and place equipment to manufacture the flexible package of Tuttle et al. may cause several problems for the flexible package. This is because

pick and place equipment uses vacuum to pick up and transfer single packages from a loading station to a workstation. During that transfer, the flexible package of Tuttle et al. may deform. This will cause intermittent contacts with testing equipment and open solder joints during the soldering process.

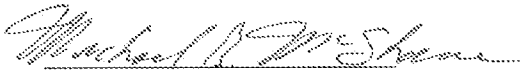
9. The Tuttle et al. package is directed toward an application where the package can be bent or flexed in an end-user product. The package taught by Quan et al. uses ceramic substrates or printed circuit board substrates that are inherently rigid. Such rigid substrates result in packages that are non-flexible and are therefore subject to breaking in the applications proposed by Tuttle et al. (See Col. 1, lines 32-35). Thus, the two packages are intended for two separate product applications, each with separate and distinct advantages.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. Executed on the date below in Austin, Texas:

Respectfully submitted,

2/17/09 .....

Date



Michael B. McShane

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.